REMARKS

The status of the claims is listed in Section A. The claim rejections are addressed in Sections B-F in the order in which they appeared in the Office Action of October 18, 2005.

A. Status of the Claims

Claims 1-9 are pending in the application. Claims 1-6 were rejected under 35 USC 112, first paragraph. Claims 1-9 were rejected under 35 USC 112, first paragraph. Claim 1 was rejected under 35 USC 102(e) as anticipated by Kuroi et al., US Patent No. 6,300,664. Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Kuroi et al. in view of Levinstein et al., UC Patent No. 4,378,628. Claims 1 and 3-9 were rejected under 35 USC 103(a) as being unpatentable over Johnson et al., US Patent No. 6,034,882 in view of Whitten et al., US Patent No. 5,451,811.

B. 35 USC 112, First Paragraph Rejections: Claims 1-6

Claims 1-6 were rejected under 35 USC 112, first paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 1 and 3-5 have been cancelled, and claim 2 has been amended to depend from claim 6.

Claim 6 has been amended to recite a semiconductor structure comprising: a first silicide layer; a silicon dioxide layer on and in contact with the first silicide layer; a first lightly doped semiconductor layer on and in contact with the silicon dioxide layer; and a second heavily doped semiconductor layer on and in contact with the lightly doped semiconductor layer, wherein the silicon dioxide layer is an antifuse layer, wherein the

antifuse layer is capable of being breached, wherein a diode is formed after the antifuse layer is breached, wherein the diode is a Schottky diode.

Applicants respectfully maintain that there can be no question whether the present application provides disclosure to enable one of ordinary skill in the art to make the claimed structure; methods to form the contiguous layerstack described are well-known. Applicants additionally maintain that disclosure to enable one of ordinary skill in the art to use the invention is provided, for example, in Fig. 5 and paragraphs [0065] through [0069], which describe rupture of the silicon dioxide antifuse layer 106 to form a Schottky diode between silicide layer 105 and n- layer 107.

That such a structure may find use in contexts other than in a railstack memory array will be apparent to those skilled in the art. Applicants can find no deficiency in enablement of claims and respectfully request reconsideration.

C. 35 USC 112, First Paragraph Rejections: Claims 1-9

Claims 1-9 were rejected under 35 USC 112, first paragraph, as failing to comply with the written description requirement. Claims 1 and 3-5 have been cancelled, and claim 2 amended to depend from claim 6.

The Examiner maintains that earlier in the specification a "vast number" of materials are disclosed as viable for both the conductor and the antifuse layer. Applicants will respectfully point out that in paragraph [0029], five materials are listed as preferred candidates for the antifuse: silicon dioxide, silicon nitride, silicon oxynitride, amorphous carbon and undoped silicon. Of the five materials, four are not mentioned again. In every subsequent mention of a material for use as the antifuse (paragraphs [0032], [0040], and [0050]), the preferred material is silicon dioxide.

In the description of the embodiment of Fig. 5, at paragraph [0069], the preferred materials for use in the conductor are aluminum, a refractory metal, or silicides. The Examiner objects that "there is no suggestion anywhere in the specification that it would be viable or appropriate to use a silicide conductor in a configuration directly abutting a silicon dioxide antifuse." Since silicon dioxide is clearly the preferred material used to form an antifuse throughout the application, and a silicide is one of the three preferred options provided for the embodiment of Fig. 5, use of a silicon dioxide antifuse adjacent to a silicide is clearly one of the most preferred embodiments suggested in the description provided.

Applicants believe the written description provides support for even a broader claim; for example for a stack in which the first two layers named are 1) a material which may be a silicide, refractory metal, or aluminum, and 2) an antifuse which may be silicon dioxide, silicon nitride, etc. That Applicants have chosen to pose a narrower claim, selecting from among the most preferred options, is Applicants' prerogative. Claim 6 does not claim or identify a particular advantage or function beyond formation of a Schottky diode upon rupture of the antifuse. This function is fully disclosed in paragraphs [0065] and [0069]. Applicants believe this disclosure demonstrates that Applicants were fully in possession of the invention at the time of filing.

Applicants respectfully request reconsideration.

D. 35 USC 102(e) Rejections: Claim 1

Claim 1 was rejected under 35 USC 102(e) as anticipated by Kuroi et al.

Claim 1 has been cancelled.

E. 35 USC 103(a) Rejections: Claim 2

Claim 2 was rejected under 35 USC 103(a) as being unpatentable over Kuroi et al. in view of Levinstein et al.

Claim 2 has been amended to depend from claim 6, rather than cancelled claim 1, from which it formerly depended. Claim 6 has been amended to include the limitations of cancelled claims 1 and 3-5, from which it formerly depended.

Thus claim 2, as amended, recites a semiconductor structure comprising: a first silicide layer; a silicon dioxide layer on and in contact with the first silicide layer; a first lightly doped semiconductor layer on and in contact with the silicon dioxide layer; and a second heavily doped semiconductor layer on and in contact with the lightly doped semiconductor layer, ***wherein the silicon dioxide layer is an antifuse layer, wherein the antifuse layer is capable of being breached, wherein a diode is formed after the antifuse layer is breached, wherein the diode is a Schottky diode,*** wherein the first silicide layer comprises cobalt silicide.

As amended, this claim includes the limitation that the silicon dioxide layer is an antifuse layer. An antifuse is an element having a function opposite that of a fuse. The antifuse initially prevents flow of current, but after being subjected to a sufficiently high voltage, the antifuse is permanently changed, allowing current to flow. Antifuses are used, for example, in memory cells to store a memory state.

The silicon dioxide layer 36 shown in Fig. 20 of Kuroi et al. is a gate dielectric, not an antifuse. In normal operation of the device of Kuroi et al., this silicon dioxide layer will not change permanently upon exposure to a high voltage and become

conductive. Thus this layer is never breached, and never forms a Schottky diode after breaching, as recited in the claim.

Applicants have shown that claim 6 distinguishes over the suggested combination. As amended, claim 2 depends from claim 6; thus Kuroi et al. combined with Levinstein et al. fail to teach each and every limitation of claim 2 as amended.

Applicants respectfully request reconsideration.

F. 35 USC 103(a) Rejections: Claims 1 and 3-9

Claims 1 and 3-9 were rejected under 35 USC 103(a) as being unpatentable over Johnson et al. in view of Whitten et al.

Claims 1 and 3-5 have been cancelled.

Claim 6 has been amended to include the limitations of cancelled claims 1 and 3-5, from which it formerly depended. As amended, claim 6 recites a semiconductor structure comprising: a first silicide layer; a silicon dioxide layer on and in contact with the first silicide layer; a first lightly doped semiconductor layer on and in contact with the silicon dioxide layer; and a second heavily doped semiconductor layer on and in contact with the lightly doped semiconductor layer, wherein the silicon dioxide layer is an antifuse layer, wherein the antifuse layer is capable of being breached, wherein a diode is formed after the antifuse layer is breached, wherein the diode is a Schottky diode.

The Examiner finds the silicide layer in Johnson et al. in conductors 46 and 50 of Fig. 6(g), which may be silicide, as may conductors 46 and 48 of Fig. 6(a). A silicon dioxide layer 42 of Fig. 6(a) is found in the same device. Lightly doped layer 41 is in contact with silicon dioxide layer 42, and heavily doped layer 40 is in contact with lightly doped layer 41.

This structure, however, shown in Fig. 6(a) of Johnson, does not include all the elements of the claim.

First, claim 3 recites a silicide layer, a silicon dioxide layer above and in contact with the silicide layer, a lightly doped layer above and in contact with the silicon dioxide layer, and heavily doped layer above and in contact with the lightly doped layer. The Examiner finds the silicon dioxide layer 42, the lightly doped layer 41, and heavily doped layer 40 in the opposite order; this portion of the structure is upside-down relative to the orientation described in the claim.

The Examiner dismisses this distinction, pointing to teaching in Johnson et al. which she maintains discloses that the orientation of the device can be changed. The Examiner points to this passage at col. 5, lines 55-65:

> ... This unidirectional behavior enables the memory decoders to establish a unique circuit path to each individual memory cell, allowing it to be individually accessed (for reads and for writes) regardless of the state of all other cells.
>
> The state change element 23 is a device which can be placed in more than one state, and whose state is not lost or altered when electrical power is removed. One possible implementation among the many discussed below, is a dielectric-rupture antifuse, having the states {high impedance} and {low impedance}. These two stored states accomplish the encoding of one bit of memory.

Applicants can find no reading of this passage that yields the Examiner's suggested interpretation; orientation is nowhere mentioned. The Examiner also points to col. 7, lines 47-57:

> Between its input terminal and output terminal, the memory cell consists of a series connection of a steering element and a state change element. In some embodiments, the steering element may be connected to the input terminal (and the state change element connected to the output terminal), and in other embodiments they may be reversed: the state change element may be connected to the input terminal and the steering element connected to the output terminal.

This passage suggests that input and output terminal can be switched. It does not say, however, that a series of layers can be vertically reversed with no effect to their function. And while it may seem logical to suggest that changing the orientation of layers should cause no change in the function of a device, in fact it is well known to those skilled in the art that changes in process may sometimes cause unexpected changes in the behavior of layers.

In addition, the claim requires a silicon dioxide layer *on and in contact with* the silicide layer. In all of the embodiments of Johnson et al. identified by the Examiner, as in Fig. 6(a), a silicon layer (for example, silicon layer 43) intervenes between the silicon dioxide layer and the silicide layer.

The Examiner uses Whitten to suggest replacing the silicon dioxide layer of the claim with silicon dioxide layer 42 *and* silicon layer 43 of Fig. 6(a) of Johnson et al. The following passage in Whitten is cited for this teaching:

> Antifuse material 20 is characterized by a high impedance but can be programmed to exhibit a low impedance by application of a suitable programming voltage. There are numerous antifuse materials available for use as antifuse element 20, including, but not limited to amorphous silicon, silicon dioxide and silicon nitride dielectric materials, or combinations of these materials. In a presently preferred embodiment of the invention, antifuse material 20 comprises amorphous silicon having a thickness of about between 0.2 to 1 micron.

Applicants must maintain that this passage in Whitten cannot be read to teach that a heavily doped polysilicon layer and a silicon dioxide layer is functionally the same as a silicon dioxide layer. First, Whitten only refers to amorphous, not polycrystalline silicon, and makes no mention of doping. This distinction is important. As will be understood by those skilled in the art, amorphous, undoped silicon is largely non-conductive, as required by an antifuse before rupture, while heavily doped, polycrystalline silicon will be conductive. The N-type dopants present in layer 43 are added to enhance conductivity.

The electrical behavior of these layers will be entirely different. As taught by Johnson et al., the purpose of analogous layer 430 is to "provide good electrical contact to the overlying conductor 480," (col. 12, lines 24-26.)

Claim 6 includes the limitation that a diode is formed after that antifuse is breached. The Examiner has not identified in Johnson et al. any sequence of layers matching those of the claim in which a diode is formed *after* rupture of the antifuse. In contrast, in the embodiment of Fig. 6(a), for example, a p-n diode already exists at the junction of layers 40 and 41 *before* the antifuse is ruptured. Rupture of antifuse layer 42 provides electrical connection between lightly doped N-type layer 41 and heavily doped N-type layer 43. The junction of these two layers, having the same conductivity type, does not form a diode.

The claim further requires formation of a *Schottky* diode upon breach of the silicon dioxide antifuse. Fig. 6(a) includes three embodiments. Only the third embodiment includes a Schottky diode, formed between layers 406 (which may be silicide) and 400, which is a lightly doped semiconductor. This embodiment also fails to anticipate the claim, however. The silicon dioxide layer 402 is not adjacent to the silicide layer 406 as in the claim, and the Schottky diode between layers 400 and 406 exists *before* the silicon dioxide antifuse 402 is ruptured.

Applicants respectfully request reconsideration.

CONCLUSION

In view of the preceding Remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicants **respectfully request an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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